

FIG. 1

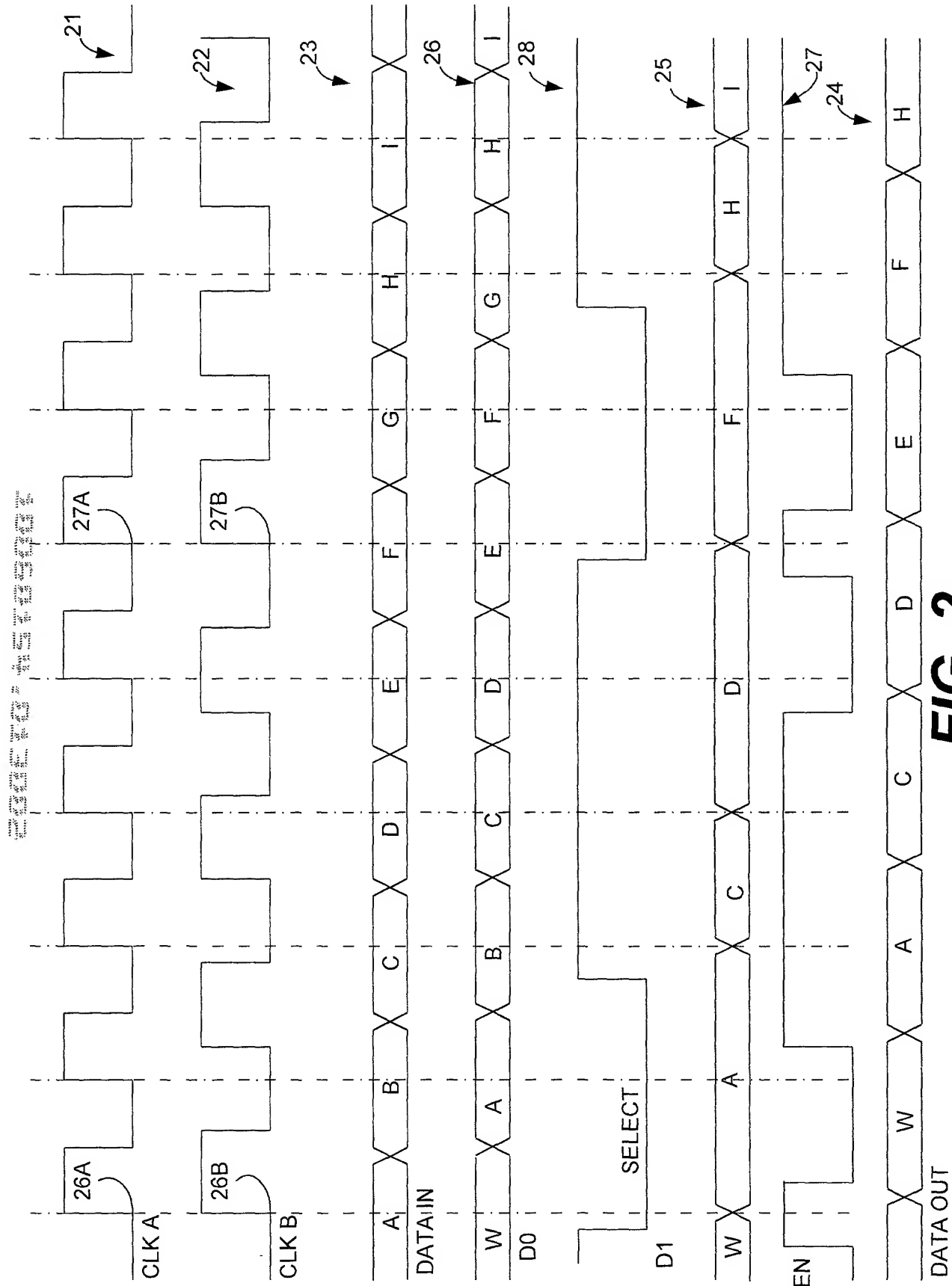


FIG. 2

FIG. 3 is a block diagram of a digital circuit 30. The circuit 30 includes a first D-type flip-flop 31, a second D-type flip-flop 32, a third D-type flip-flop 33, a fourth D-type flip-flop 34, a fifth D-type flip-flop 35, a first 2-to-1 multiplexer 36, a second 2-to-1 multiplexer 37, and a third 2-to-1 multiplexer 38. The circuit 30 is configured to perform a data shift operation. The first D-type flip-flop 31 has a DATA IN input and a CLOCK B input. The second D-type flip-flop 32 has a Q output connected to the D input of the third D-type flip-flop 33. The third D-type flip-flop 33 has a Q output connected to the D input of the fourth D-type flip-flop 34. The fourth D-type flip-flop 34 has a Q output connected to the D input of the fifth D-type flip-flop 35. The fifth D-type flip-flop 35 has a Q output connected to the D input of the first D-type flip-flop 31. The first 2-to-1 multiplexer 36 has a SELECT input and two data inputs, D0 and D1. The second 2-to-1 multiplexer 37 has a SELECT input and two data inputs, D0 and D1. The third 2-to-1 multiplexer 38 has a SELECT input and two data inputs, D0 and D1. The circuit 30 is configured to perform a data shift operation. The first D-type flip-flop 31 has a DATA IN input and a CLOCK B input. The second D-type flip-flop 32 has a Q output connected to the D input of the third D-type flip-flop 33. The third D-type flip-flop 33 has a Q output connected to the D input of the fourth D-type flip-flop 34. The fourth D-type flip-flop 34 has a Q output connected to the D input of the fifth D-type flip-flop 35. The fifth D-type flip-flop 35 has a Q output connected to the D input of the first D-type flip-flop 31. The first 2-to-1 multiplexer 36 has a SELECT input and two data inputs, D0 and D1. The second 2-to-1 multiplexer 37 has a SELECT input and two data inputs, D0 and D1. The third 2-to-1 multiplexer 38 has a SELECT input and two data inputs, D0 and D1. The circuit 30 is configured to perform a data shift operation.

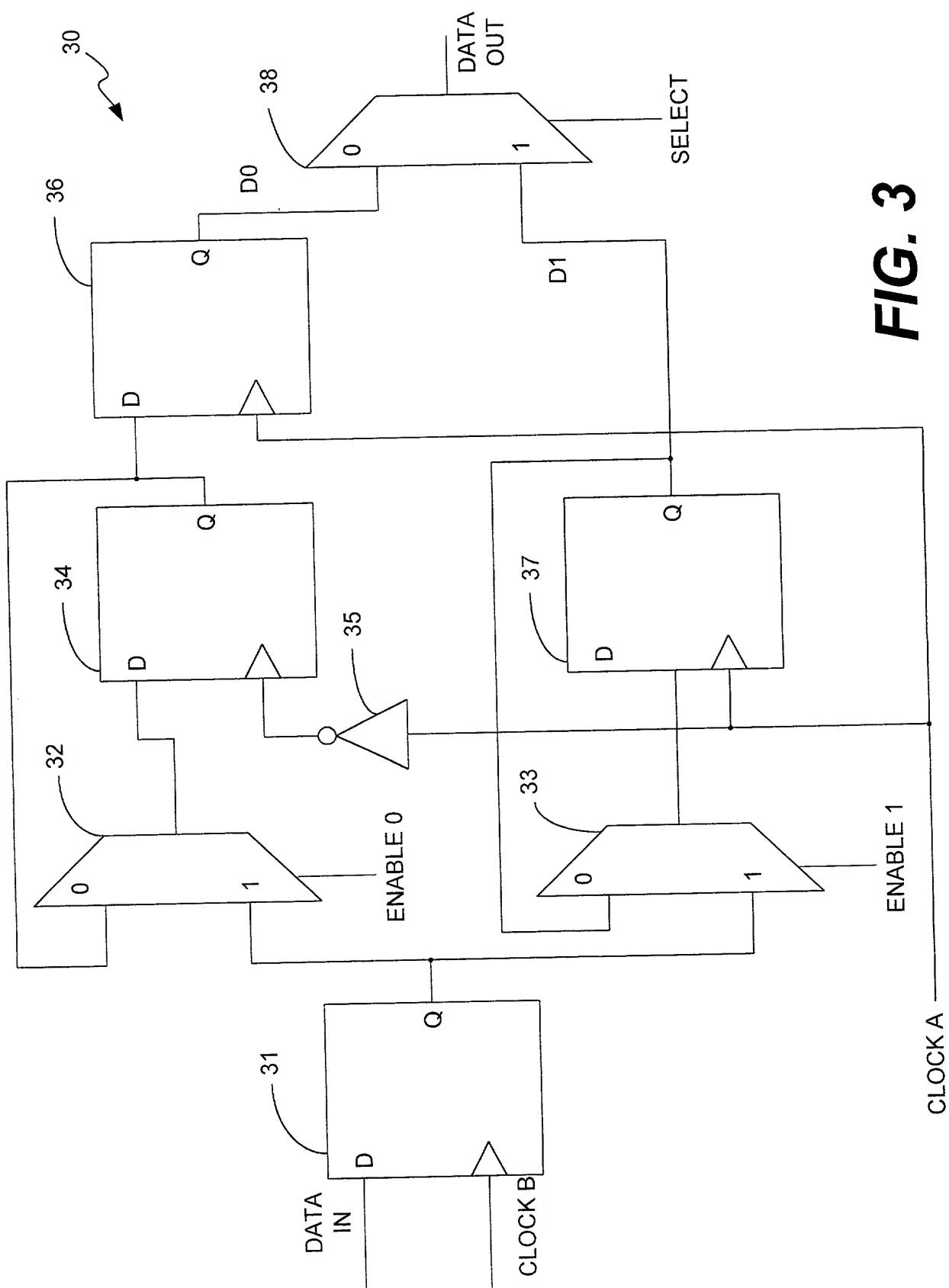


FIG. 3

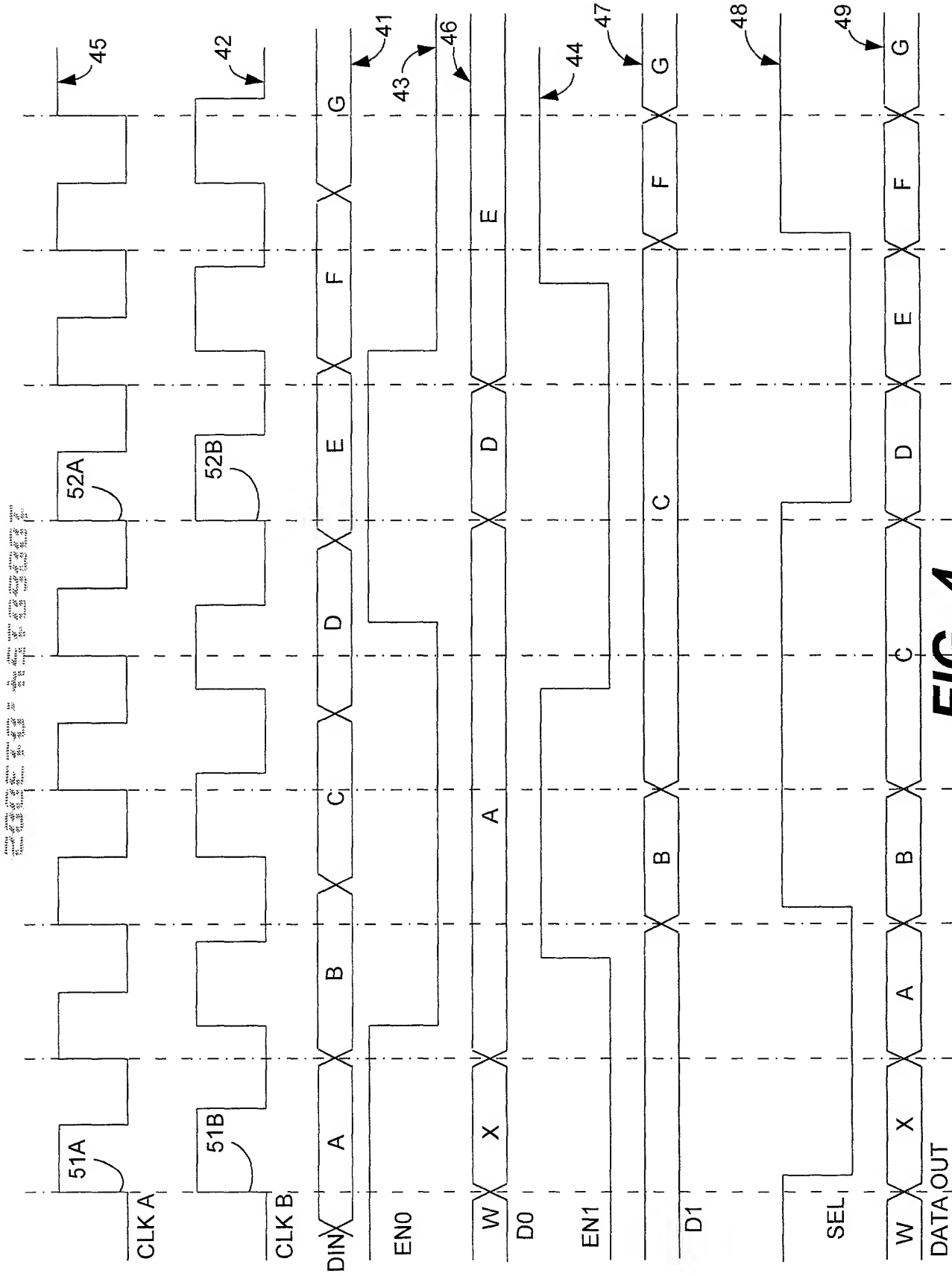


FIG. 4